MEDEA+ TOOLIP/MESA Workshop

Complex SoC Design Methodologies and Experiments

World Trade Center, room Cervin - Grenoble - November 14, 2003

9:00 – 12:00 **Organizer:** STMicroelectronics
Chairman: Joseph Borel, J.B R&D Consulting

Introduction

This cooperative workshop aims at showing illustrative achievements obtained in the frame of TOOLIP (2001-2003) and MESA (2001-2004), two MEDEA+ projects contributing together, with a total of 46 partners, to today's largest European initiative on high-level design techniques. The common goal is to provide consistent design flows to allow building, validating and assembling complex, parametric and reusable Intellectual Property (IP) cores. While TOOLIP focuses on methodologies and tools for reusability, MESA puts specific stress on architectures for multi-processor and HW/SW codesign.

Due to increasing gate density, it is commonly said that volume of data to handle is getting huge: however, stronger bottlenecks tend to appear to validate and verify design descriptions (prohibitive computation time) and to handle on-chip communication (limited bandwidth).

Four talks on *Validation and Verification* and two talks on *On-Chip Networking*, will address different levels of the design flow (algorithmic, HW, SW, HW/SW) and propose promising ways to bypass or alleviate these bottlenecks.

Validation and Verification

"Early embedded Software development and IP validation using SoC TLM platforms"

Stéphane Curaba, Laurent Maillet-Contoz, STMicroelectronics

The growing complexity of the SoCs calls for new and efficient specification and design methodologies. A key point to reduce the time to market is the early validation of the functional specifications, as well as an early development of the embedded software. We present a simulation environment based on the Transaction Level Modeling (TLM) approach developed within ST, introduce the main concepts and give an overview of the simulation infrastructure built on top of SystemC 2.0. We illustrate this approach on a real example.

"High-level modeling of software IP components and RTOS using SystemC"

Wander Cesario, TIMA Laboratory

We present a prototype environment for software IP validation using high-level modeling of software IP components and RTOS in a SystemC. The goal is to provide a cosimulation environment for HW/SW IP co-validation, where the software part is modeled at the operating system level, whereas the hardware part may be modeled at different abstraction levels (e.g., transaction, RT-level). The simulation environment provides an abstract RTOS model that allows measuring architecture performances. It uses a hierarchical scheduler library that extends SystemC HW-only scheduling scheme for the simulation of RTOS scheduling, I/O, and IT services.

Software IP simulation is achieved using an adaptation layer representing the operating system. We use a hardware abstraction layer (HAL) that enables to split the RTOS model into two parts: one that is dependent on the processor local architecture (the HAL part) and other that is not. This scheme was used for the modeling of a generic RTOS, the OS generated by TIMA tools and eCos (an open-source embedded OS).

“Assertion-Based Verification (ABV) of IP/SoC”

H.N. Nguyen, Bull

In relation with Design Reuse, Verification should be re-defined the same way to cope with the increasing complexity and size of today’s designs. Traditional methods based on a set of ad-hoc test benches and monitoring techniques for simulation are no longer efficient and hence should be reshaped with new structures and new methodologies to provide re-usability (gain in efficiency) in association with the re-use design methodology and to enable the adoption of re-emerging (semi-) formal techniques.

The focus of this presentation is three-fold:

The purpose of Verification Reuse is to provide a methodology that will enable the functional checking across a wide variety of tools ranging from Formal Verification to Simulation and Emulation. ABV will be applied to the verification and integration of IPs while implementation modes will be chosen according to the subsequent processing methods (dynamic / static verification).

"Automatic detection of run-time errors extended to embedded DSP and micro-controllers"

Daniel Pilaud, PolySpace Technologies

Runtime errors are particularly difficult to identify, and located at the edge between Hardware and Software. In parallel with HW verification, SW verification appears to be a new necessary step of the design flow, to allow run-time errors detection prior to code freezing. The definition of a systematic method is necessary to seek latent faults that may cause non-determinism, incorrect results or processor halt. PolySpace Technologies has developed a unique solution to automate the detection of these types of errors. In cooperation with STMicroelectronics, Polyspace has extended this environment to the analysis of microcontroller and DSP code. This talk will present the results and future perspective of this work.

On-Chip Networking

“Concepts and implementation of the Philips Network-on-Chip”

John Dielissen, Philips

Standard communication protocols (e.g. DTL and AXI) and services are essential to reuse IPs in Systems on a Chip (SoC). SoC communication infrastructures, such as the Aethereal network on chip (NoC), play a central role in integrating IPs with diverse communication requirements. We believe that the provision of guaranteed services (e.g. throughput and latency) is essential for compositional and predictable system design. A router network implements basic services, while service differentiation is provided by the network interfaces. To be cost effective, most, if not all, of the services have to be implemented in hardware.

We illustrate this with our modular network interface architecture, which seamlessly connects IPs, using their native protocols such as DTL or AXI. For programmable SoCs, run-time NoC reconfiguration is important. We show how the Aethereal NoC achieves this, using the NoC itself, instead of an additional control network.

“Performances evaluations of the SPIN micro-network”

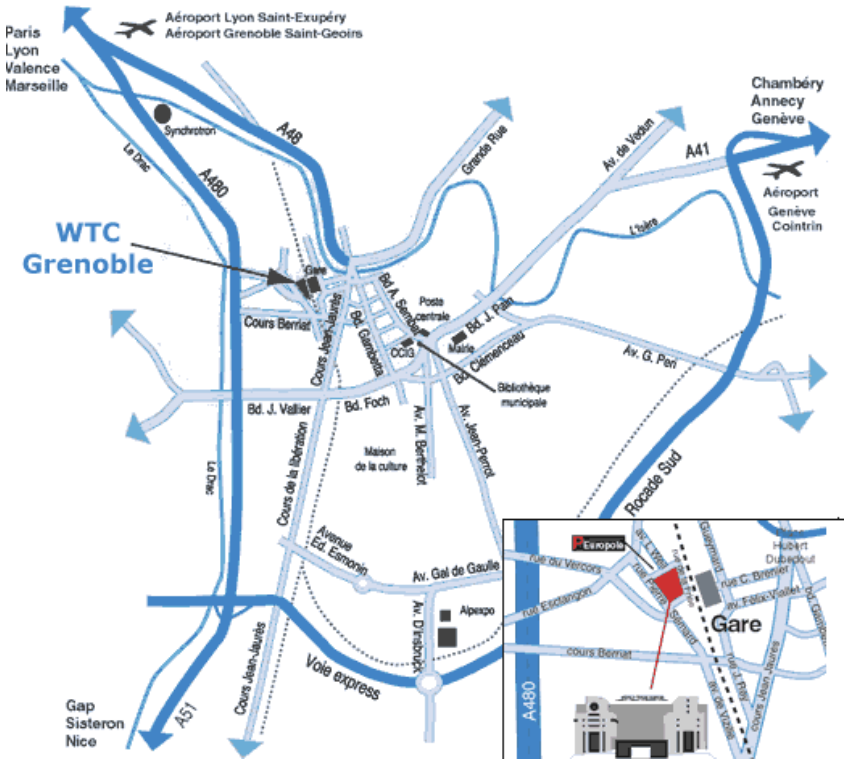
Alain Greiner, LIP6/UPMC

The architectural interconnection of a large number of cores is getting increasingly a bottleneck in System-on-Chip design, as bus-based interconnects will not scale to support throughputs in the 10-100 Gbit/s. Focusing on a very promising technique for on-chip communication, LIP6/UPMC has built a 5-year expertise on SPIN (Scalable, Programmable, Integrated Network). SPIN is a toolbox of macro-cells and methods for fast design of low-cost, high-performance and scalable interconnections for SoCs. The core technology is a packet-switched multi-stage network.

The work under way at LIP6/UPMC aims at developing, in close cooperation with Philips and ST, simulation models of the SPIN network. During the talk, systematic performance comparisons between the SPIN micro-network and a classical PIBUS will be presented.

Location:	World Trade Center, 5 place Robert Schuman, 38 000 Grenoble, FRANCE 5' from railway/TGV station and from bus shuttles with Lyon airport
Registration:	Simply email your coordinates to Deborah.Lalomia@st.com with subject "Registration to TOOLIP/MESA Workshop"
Fees:	This is a public workshop with free access. Registration is mandatory.

Access map - Accomodations



Hotels near *World Trade Center (WTC)*, Grenoble :

NOVOTEL WORLD TRADE CENTER ***
7 place Robert Schuman - 38 000 Grenoble
Phone : +33 4.76.70.84.84 - Fax : +33 4.76.70.24.93
Internet : http://www.accorhotel.com
e-mail : H1624@accorhotel.com

HOTEL EUROPOLE ***
29, rue P. Sémard
38000 GRENOBLE
Phone : 04 76 49 51 52 - Fax : 04 76 21 99 00

HOTEL SUISSE ET BORDEAUX **
6, place de la Gare - 38 000 Grenoble
Phone : +33 4.76.47.55.87 - Fax : +33 4.76.46.23.87
Internet : http://www.hotel-sb-grenoble.com/
e-mail : info@hotel-sb-grenoble.com

HOTEL TERMINUS ***
10, place de la Gare - 38 000 Grenoble
Phone : +33 4.76.87.24.33 - Fax : +33 4.76.50.38.28
Internet : http://www.terminus-hotel-grenoble.fr
e-mail : terminush@aol.com

HOTEL TOURING **
26 Avenue Alsace Lorraine - 38000 Grenoble
Phone +33 4 76 46 24 32 - Fax +33 4 76 46 02 85

HOTEL TERMINUS**
10 Place de la Gare - 38000 Grenoble
Phone +33 4 76 87 24 33 - Fax +33 4 76 50 38 28

HOTEL DES ALPES **
45 avenue Felix Viallet - 38000 Grenoble
Phone +33 4 76 87 00 71 - Fax +33 4 76 56 95 45

HOTEL BASTILLE **
25 avenue Felix Viallet - 38000 Grenoble
Phone +33 4 76 43 10 27 - Fax +33 4 76 87 52 69